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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,114	02/20/2001	Pin-Shyne Chin	TS00-338	4177

28112 7590 12/03/2002

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EXAMINER
BEREZNY, NEAL

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,114	CHIN ET AL.	
	Examiner	Art Unit	
	Neal Berezny	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 15, at the end of step e, the limitation "said cell node region" appears to be incomplete. It is not clear what this limitation is meant to convey. Is the cell node region also adjacent to the bitline region?

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilgen et al. (5,134,085). Gilgen teaches a method of fabrication of a DRAM, comprising the steps of forming a word line structure and a capacitor plate structure on a substrate; fig.16, el.101, 161,a capacitor plate structure comprised of a capacitor dielectric formed on said substrate, el.152, col.8, ln.34-38, and a conductive plate layer formed on said capacitor dielectric; el.161, patterning the conductive and dielectric layers to form a word line and a capacitor plate

structure, fig.10, el.71 and 103, fig.15 and 16, el.154, 161, and 152, said capacitor plate structure overlying a plate region of said substrate; el.151, said plate region and said conductive plate layer acting as plates of a capacitor; implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure,el.112, said cell node region; forming spacers on the sidewalls of said word line structure and said capacitor plate structure; el.171, 161, forming a mask pattern over said cell node; el.154, implanting ions of a first conductivity type into said substrate to form a second bitline region; Fig.17, and not implanting ions into said cell node; removing the mask pattern; col.8, ln.59-65, forming a dielectric layer over said substrate; fig.19, el.192, and forming a bitline contact to said second bitline region, fig.20, el.201. Gilgen does not teach performing the first implant step after the formation of the wordline and capacitor plate structures, but rather before their completions. It would be obvious to one of ordinary skill in the art at the time of the invention to modify Gilgen to spread out the capacitor structure and separate it from the cell node region and perform the first implant later in order to reduce leakage currents. Giligen's structure is designed to use

less area, but at the expense of higher leakage currents and it would be obvious to employ either design based on the demands placed on the device.

5. Claims 2, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilgen as applied to claim 1 above, and further in view of Mandelman et al. (6,274,441). Gilgen does not specifically state that the second bit line region 60 preferably has an impurity concentration greater than the cell node region 40 by at least a factor of 10, nor wherein said second bitline region has a concentration between 1E20 and 1E21 atom/cc, nor wherein said first bit line region has a p-type doping and has an impurity concentration between 1E18 and IE 19 Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region has a p-type doping and has an impurity concentration between 1E18 and 1E19 atom/cc. Mandelman teaches that the second bit line region preferably has an impurity concentration greater than the cell node region 40 by at least a factor of 10, see claim 8 and col.3, ln.43-51, wherein said second bitline region has a concentration between 1E20 and 1E21 atom/cc, claim 8, wherein said first bit line region has a p-type doping and has an impurity concentration between 1E18 and IE 19 Atoms/cc, col.3, ln.43-51, said second bit line region has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region has a p-type doping and has an impurity concentration between 1E18 and 1E19 atom/cc. It would be obvious to one of ordinary skill in the art at the time of the invention to employ well known dopant concentration analysis to determine these dopant profiles to achieve

the desired device characteristics, so as to increase switching speeds, lower resistance, and improve device performance. Further it is well known in the art to interchange N-type devices for P-type devices and visa versa, see Gilgen, col.1, ln.51-58. It would be obvious to one of ordinary skill in the art at the time of the invention to switch dopant types to increase the latitude of device characteristics and performance features, such as those found in CMOS devices.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilgen and Mandelman as applied to claims 1-2, 5-7 above, and further in view of Chi (6,262,447). Gilgen and Mandelman appear not to specifically state that the substrate is doped with an n-type impurity; having an impurity concentration between 1E17 and 1E18 atoms/cc, nor that the substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between 1E17 and 1E18 atoms/cc. Chi teaches forming a P-well for an N-type device, with an impurity concentration between 1E17 and 1E18 atoms/cc, col.2, ln.60-62. It would be obvious to one of ordinary skill in the art at the time of the invention to employ well known dopant concentration analysis to determine these dopant profiles to achieve the desired device characteristics, so as to increase switching speeds, lower resistance, and improve device performance. Further it is well known in the art to interchange N-type devices for P-type devices and visa versa, see Gilgen, col.1, ln.51-58. It would be obvious to one of ordinary skill in the art

at the time of the invention to switch dopant types to increase the latitude of device characteristics and performance features, such as those found in CMOS devices.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gilgen, Mandelman, and Chi as applied to claims 1-7 above, and further in view of Wolf, vol.2, p.589. Gilgen, Mandelman, and Chi do not appear to specifically state that the cell node region and said first bit line region do not intersect. Wolf teaches that the cell node region and said first bit line region do not intersect, p.589, fig.8-10 (b&c). It would be obvious to one of ordinary skill in the art at the time of the invention to form the cell node region and the first bit line region so as not to intersect, in order to reduce leakage currents between the regions, thereby increasing performance.

Response to Arguments

8. Applicant's arguments filed 10/11/02 have been fully considered but they are not persuasive. Applicant alleges differences between claim 1 and Gilgen based on the assertion that various components are not formed on the **substrate,** and that spacers are not formed on the **capacitor plate structure**. Applicant is reminded that the Examiner is required to interpret the claims as broadly as reasonably possible. The substrate could be interpreted as including the bottom polysilicon capacitor plate. Further, the spacers (171) are on the word line sidewalls and the capacitor plate (161) also serves as a spacer on the sidewall of the capacitor structure since it covers the sidewalls of the bottom capacitor plate, which is considered part of the capacitor

structure. Applicant also makes assertions of non-obviousness based on these alleged differences, but provides no support for such an assertion. Merely a difference does not constitute non-obviousness. Further, applicant argues that Gilgen does not form a 1T SRAM, but such an element is not found in the claims. Note, this element has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

9. Applicant argues that switching dopant types is not obvious. Applicant is directed to Gilgen, col.1, ln.51-58. Further, switching and altering dopant types and concentrations have been extensively studied in the art for decades and applicant has failed to identify either in the specifications or in the response, any critical or unexpected results arising from such alleged modifications. Applicant's attention is also directed to claim 8 and not claim 18 in Gilgen. Further, examiner need not have the same reasons for combining as applicant's. Examiner has cited the motivation for combining in the rejection to reduce electrical resistance of the bitline.

10. The rest of applicant's arguments depend on the assertion that the parent claims as amended are allowable, which examiner has rejected.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on M-F 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)

308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NB
November 24, 2002

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800